AMENDMENTS

In the Specification

Please amend the following paragraphs as indicated:

(for the paragraph beginning at page 6, line 10)

The present invention provides a high voltage device comprising a substrate of a first type, [[a]] first and second [[well]] wells respectively of the first type and a second type in the substrate, a gate formed on the substrate, [[a]]first and second doped ~~region~~ regions both of the second type, respectively formed in the first and second [[well]] wells and both sides of the gate, and a third doped region of the first type in the first well and adjacent to the first doped region.

(for the paragraph beginning at page 6, line 18)

The present invention provides a second high voltage device formed on a P substrate comprising an HVNMOS and a HVPMOS. The HVNMOS comprises [[a]] first P and N [[well]] wells in the P substrate, a first gate formed on the P substrate, two first N+ doped regions respectively formed in the first P and N [[well]] wells, and both sides of the first gate, and a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well. The HVPMOS comprises an N+ buried layer in the P substrate, [[a]] second N and P [[well]] wells in the P substrate and above the N+ buried layer, a second gate formed on the P, two second P+ doped regions respectively formed in the second N and P [[well]] wells, and both sides of the second gate, and a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well.

(for the paragraph beginning at page 7, line 4)

The present invention further provides a first method for manufacturing a high voltage device, comprising the steps of providing a substrate of a first type, forming [[a]] first and second [[well]] wells respectively of the first type and a second type in the substrate, forming a gate on the substrate, forming [[a]]first and second doped ~~region~~ regions both of the second type, respectively in the first and second [[well]] wells and both sides of the gate, and forming a third doped region of the first type in the first well and adjacent to the first doped region.

(for the paragraph beginning at page 7, line 14)

The present invention further provides a second method for manufacturing a high voltage device comprising the steps of providing a P substrate, forming a HVNMOS on the P substrate by forming [[a]] first P and N [[well]] wells in the P substrate, forming a first gate on the P substrate, forming two first N+ doped regions respectively in the first P and N [[well]] wells, and both sides of the first gate, and forming a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well, and forming a HVPMOS on the P substrate by forming an N+ buried layer in the P substrate, forming [[a]] second N and P [[well]] wells in the P substrate and above the N+ buried layer, forming a second gate on the P substrate, forming two second P+ doped regions respectively in the second N and P [[well]] wells, and both sides of the second gate, and forming a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well.

(for the paragraph beginning at page 8, line 20)

FIG. 4 is a cross-sectional schematic diagram of the HVNMOS transistor formed on a P substrate 400 according to one embodiment of the invention. As shown in FIG. 4, a P well 411 and N well 412 are formed in the P substrate 400. A gate structure 420 is formed on the P substrate 400 and includes a gate oxide 421 on the P substrate 400, a conducting layer (poly-silicon) 422 on the gate oxide 421 and spacers 423 on two sides of the gate oxide 421 and conducting layer 422. ~~A first~~ First and second N+ doped ~~region~~ regions 431 and 432 are respectively formed in the P well 411 and N well 412, and both sides of the gate structure 420. An N lightly doped region 433 is formed adjacent to the first N+ doped region 431 and beneath one of the spacers 423. A P doped region 440 is formed in the P well 411 and adjacent to the first N+ doped region 431. Field oxides 450 isolate the HVNMOS transistor from other devices on the P substrate 400. The doped regions 440 and 431 form the source of the HVNMOS transistor while the doped region 432 forms the drain of the HVNMOS transistor. The spacing of the second N+ doped region 432 to the edge of the gate structure 420 should be an appropriate value so that the drain side of the HVNMOS sustains a high breakdown voltage. The overlay of the gate structure 420 and the N well 412 is defined as zero.

(for the paragraph beginning at page 9, line 14)

FIG. 5 is a cross-sectional schematic diagram of the HVPMOS transistor made on a P substrate 500 according to one embodiment of the invention. As shown in FIG. 5, an N well 511 and P well 512 are formed in the P substrate 500. A gate structure 520 is formed on the P substrate 500 and includes a gate oxide 521 on the P substrate 500, a conducting layer (poly-silicon) 522 on the gate oxide 521 and spacers 523 on two sides of the gate oxide 521 and

conducting layer 522. ~~A first~~ First and second P+ doped ~~region~~ regions 531 and 532 are respectively formed in the N well 511 and P well 512, and both sides of the gate structure 520. A P lightly doped region 533 is formed adjacent to the first P+ doped region 531 and beneath one of the spacers 523. An N doped region 540 is formed in the N well 511 and adjacent to the first P+ doped region 531. Field oxides 550 isolate the HVPMOS transistor from other devices on the P substrate 500. The doped regions 540 and 531 form the source of the HVPMOS transistor while the doped region 532 forms the drain of the HVPMOS transistor. The spacing of the second P+ doped region 532 to the edge of the gate structure 520 should be an appropriate value so that the drain side of the HVPMOS sustains a high breakdown voltage. The overlay of the gate structure 520 and the P well 512 is defined as zero. It should be noted that an N+ buried layer 560 is formed beneath the N well 511 and P well 512 for isolation of the P well 512 from the P substrate 500. Further, due to the formation of the N+ buried layer, a P epitaxial layer 570 is formed in the substrate 500. Typically, the HVNMOS and HVPMOS are formed on the same wafer with the same processing steps. The P epitaxial later 570 is also formed in the HVNMOS side of the substrate 400, as shown in FIG. 4.

(for the paragraph beginning at page 10, line 18)

As shown in FIG. 6A, the high voltage device is formed on a P substrate 600 and includes [[a]] HVNMOS and HVPMOS ~~transistor~~ transistors on different regions of the P substrate 600. The HVNMOS transistor will be formed on the left and HVPMOS on the right. An N+ buried layer 610 is formed in the P substrate 600 on the HVPMOS region. The N+ buried layer 610 is essential to the HVPMOS transistor for isolating the P well 642 from the P substrate 600. Those skilled in the art will appreciate that formation of the N+ buried layer 610 inherently results in

formation of a P epitaxial layer 620 in the P substrate 600. Since the P epitaxial layer 620 is formed globally in the substrate 600, it also appears in the HVNMOS region although it is not essential for the HVNMOS transistor.

(for the paragraph beginning at page 11, line 11)

As shown in FIG. 6C, a local oxidation process is performed to form field oxide regions 650. The field oxide regions 650 define active regions for the HVNMOS and HVPMOS ~~transistor~~ transistors, which isolate the HVNMOS and HVPMOS transistors from other devices on the P substrate 600.

(for the paragraph beginning at page 12, line 15)

As shown in FIG. 6F, N+ doped regions 681, 682 and 693, and P+ doped regions 683, 691 and 692 are formed in the P substrate 600 by two ion implantation steps. For the N+ doped regions 681, 682 and 693, the first ion implantation step uses phosphorous ion as a dopant while the second ion implantation step uses boron ion as a dopant to form the P+ doped regions 683, 691 and 692. It should be noted that the spacing of the N+ doped region 682 to the edge of the gate structure 660, and the P+ doped region 692 to the edge of the gate structure 660 must be properly defined. If the N+ doped region 682 and the P+ doped region 692 are too close to the edge of the gate structure 660, the drain sides of the HVNMOS and HVPMOS ~~transistor~~ transistors will suffer a low breakdown voltage.